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CLAIMS

1. An apparatus comprising:

a first logic circuit comprising one or more counters and configured to synchronize a plurality of input clock signals; and
a second logic circuit configured to detect and present
5 a faster clock signal of said synchronized clock signals.

2. The apparatus according to claim 1, wherein said

first logic circuit comprises digital fast clock detection circuit.

3. The apparatus according to claim 1, wherein said one

or more counters comprise saturation counters.

4. The apparatus according to claim 1, wherein said

second circuit comprises:

a fast clock detect circuit with programmable resolution configured to control a resolution of said apparatus.

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5. The apparatus according to claim 4, wherein said fast clock detect circuit is enabled or disabled in response to one or more configuration bits.

6. The apparatus according to claim 5, wherein said fast clock detect logic, when disabled, is configured to be by-passed by a programmable configuration bit.

7. The apparatus according to claim 1, wherein said apparatus is configured to synchronously select said faster clock signal.

8. The apparatus according to claim 1, wherein said apparatus is fully configurable.

9. The apparatus according to claim 1, wherein said apparatus is configured to provide programmable resolution.

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10. The apparatus according to claim 9, wherein said programmable resolution is configured to be increased or decreased by adjusting a count value.

11. The apparatus according to claim 1, wherein said apparatus is configured to provide automatic detection and configuration of one or more devices to said faster clock signal.

12. The apparatus according to claim 1, wherein said apparatus is configured to control one or more first-in first-out (FIFO) memories using a single port memory.

13. The apparatus according to claim 1, wherein said apparatus is configured to control one or more multiqueue memories using a single port memory.

14. The apparatus according to claim 1, wherein said apparatus is configured to control one or more multiport memories using a single port memory.

15. The apparatus according to claim 1, wherein:
said first logic circuit comprises a faster clock detect
circuit configured to synchronize said plurality of input clock
signals; and

5 said second logic circuit comprises a configuration
resolution circuit configured to control a resolution of said
apparatus, a configuration circuit configured to control a
selection of said faster clock signal and a select circuit
configured to select said faster clock signal.

16. An apparatus comprising:
means for synchronizing a plurality of input clock
signals with one or more counters; and
means for detecting and presenting a faster clock signal
5 of said synchronized clock signals.

17. A method for selecting a clock signal, comprising
the steps of:

(A) synchronizing a plurality of input clock signals
with one or more counters; and

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5 (B) detecting and presenting the faster clock signal of
said synchronized clock signals.

18. The method according to claim 17, further comprising
the step of:

controlling resolution in response to one or more
configuration bits.